XFT Review

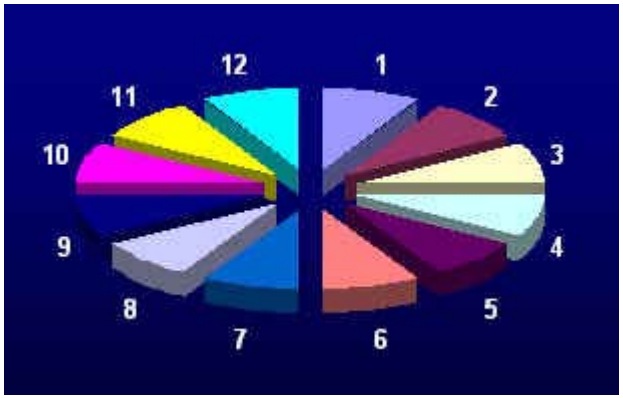
XFT Review
Stereo Finder Design

T. Shaw

Stereo Finder

Stereo Finder

- Plan to instrument SL3,SL5, and SL7
- Each Finder will cover a 30˚ section
- Each SL will require 12 Stereo Finders, for a total of 36 production boards.

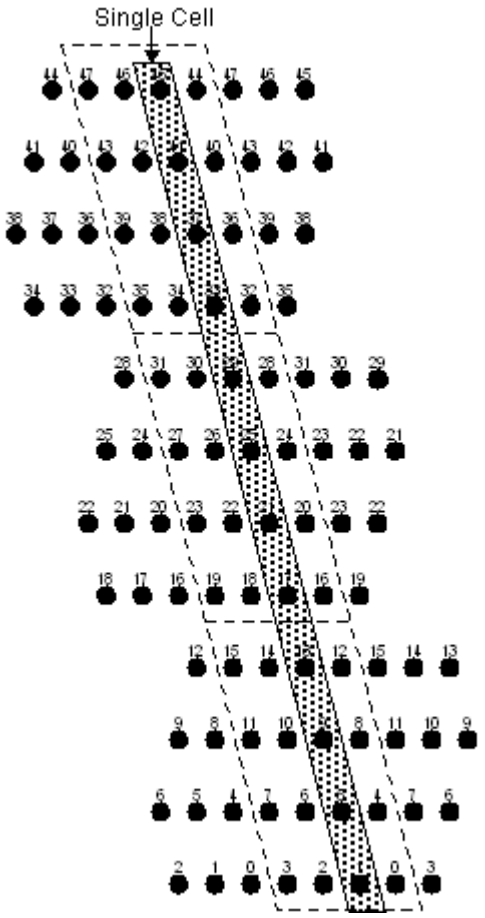


Finder Inputs

A Finder "cell" is defined as a group of 12 TDC wires.

Previous Finder algorithms worked off a "core" of 4 cells plus neighbors.

4 cells represent data from 48 wires, or half a TDC.



Scope

Finder algorithm is now being studied to determine how many cells can be handled in a single FPGA. Working number for now is 4 cells per FPGA.

	# of Finder Cells in COT layer	# of 4 cell cores/FPGAs in COT layer	# of cores/FPGAs required for 30˚
SL7	432	108	9
SL5	336	84	7
SL3	240	60	5

TDC Inputs

- The source of the XFT data are TDC modules.
- These modules contain timing information for 96 wires.
- The TDC will produces 6 bits of data (6 time slices) for each wire.
- This data identifies whether a wire has a “hit” on it for a particular time slice.
- There are 6 identified time slices within each 396ns period, or 3 CDF_Clock cycles.

TDC Inputs

In addition to sending up the hit information for each wire, it is desirable to tag the information with a Beam_Zero marker, to identify its position in time as well as some type of identification tag to mark the source of the data.

TDC Inputs

Current plan is to send the data from the TDC modules to the XFT modules via an 8B/10B encoded serial optical bitstream.

Furthermore, we would like to limit the data rate on such a link to ~1.25Gbps which is supported by a wide variety of commercial products available for Gigabit Ethernet.

Data Packing using 16 bit Serializer

Data Fiber # 1 carries information from TDC wires 0-47

Data Word	Beam_Zero Marker 1 bit	Word Zero Flag 1 bit	Group Identifies 2 bits	Wire data time slice (0-5) 12 bits
1	beam_zero	1	00	t0 (0-11)
2	beam_zero	1	01	t0 (12-23)
3	beam_zero	1	10	t0 (24-35)
4	beam_zero	1	11	t0 (36-47)
5	beam_zero	0	00	t1 (0-11)
6	beam_zero	0	01	t1 (12-23)
7	beam_zero	0	10	t1 (24-35)
8	beam_zero	0	11	t1 (36-47)
9	beam_zero	0	00	t2 (0-11)
10	beam_zero	0	01	t2 (12-23)
11	beam_zero	0	10	t2 (24-35)
12	beam_zero	0	11	t2 (36-47)
13	beam_zero	0	00	t3 (0-11)
14	beam_zero	0	01	t3 (12-23)
15	beam_zero	0	10	t3 (24-35)
16	beam_zero	0	11	t3 (36-47)
17	beam_zero	0	00	t4 (0-11)
18	beam_zero	0	01	t4 (12-23)
19	beam_zero	0	10	t4 (24-35)
20	beam_zero	0	11	t4 (36-47)
21	beam_zero	0	00	t5 (0-11)
22	beam_zero	0	01	t5 (12-23)
23	beam_zero	0	10	t5 (24-35)
24	beam_zero	0	11	t5 (36-47)

Optical Fiber Rates

If the data is packed as in the previous example,

We would need a data rate of:

20 encoded bits/16 data bits x 16 data bits x 24 words ÷ 396ns = 1.21 Gbps

This would require a Serdes clock period of 16.5 ns

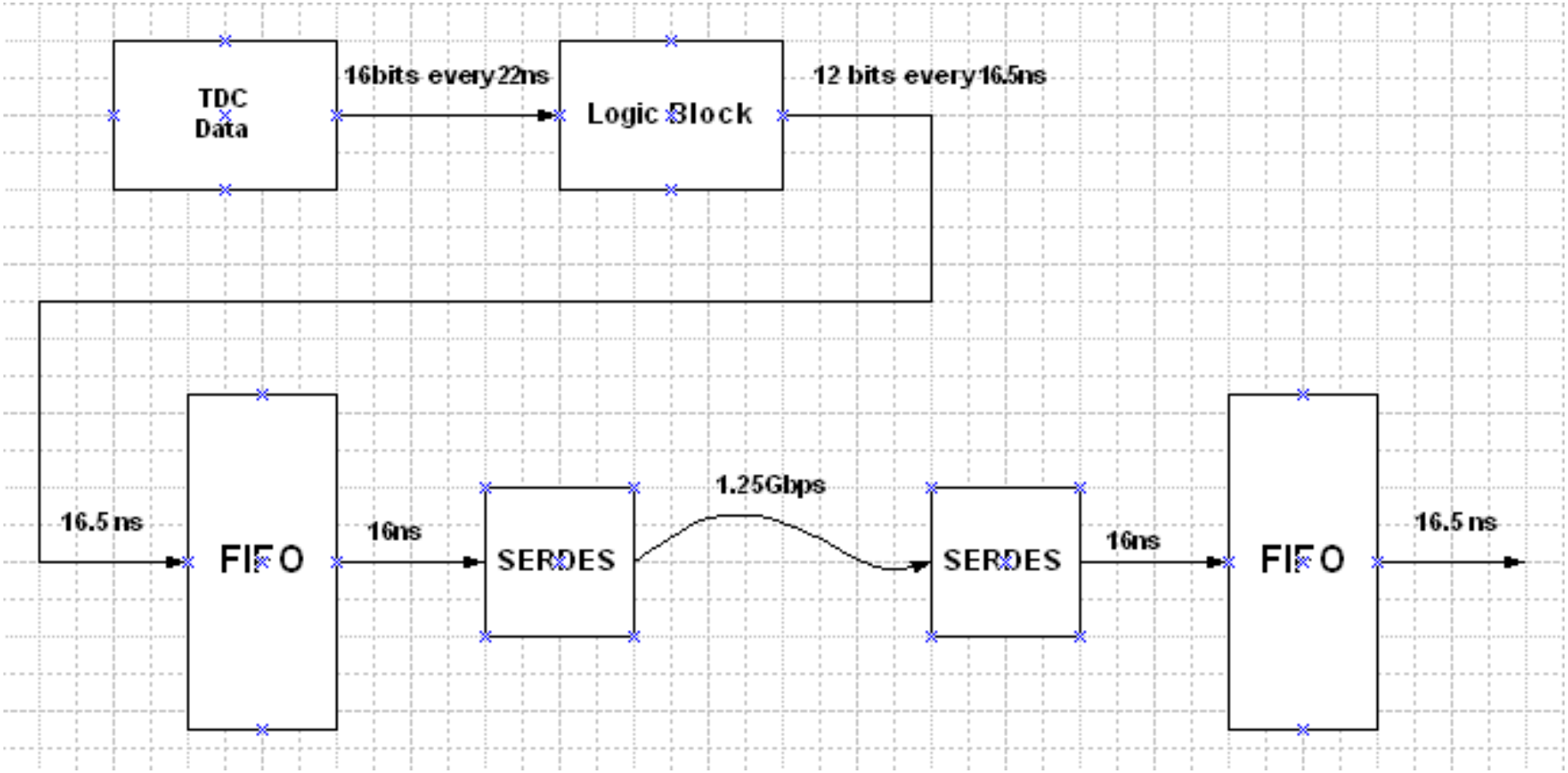
(CDF_Clock ÷ 8)

The recommended clock jitter of the Serdes parts is ~40ps pk-pk. It would be very difficult to achieve this with detector clock. We may run the links with 62.500 MHz oscillator which is slightly faster (16ns clock period) than CDF_Clock ÷ 8.

-> some kind of buffer/FIFO to smooth out clock differences

Data flow TDC-> Finder

XFT Upgrade



O/E and E/O Examples

XFT Upgrade

Dual Receivers

M2R-25-4-1-TL Optical Gigabit Ethernet/Fibre Channel
850nm SFF 2x5 Dual Receivers -- 1.25/1.0625GBaud --- +3.3V

Features

- 1.25 Gbps Gigabit Ethernet Compliant
- Metalized Plastic Package
- TTL Signal Detect output
- AC coupled PECL level outputs
- Low profile fits Mezzanine Card Applications
- Single +3.3V Power Supply
- Wave Solderable / Aqueous Washable
- Class 1 Laser Safety Compliant
- UL 1950 Approved

PRODUCT OVERVIEW

The M2R-25-4-1-TL Small Form Factor (SFF) optical dual receiver modules are high performance integrated duplex data links for uni-directional communication over multimodeoptical fibre. The M2R-25-4 module is

Dual Transmitters

M2T-25-4-1-L Optical Gigabit Ethernet/Fibre Channel
850nm SFF LC 2x5 Dual Transmitters - 1.25/1.0625GBaud -- +3.3V

Features

- 1.25 Gbps Gigabit Ethernet Compliant
- 1.0625Gbps Fibre Channel Compliant
- Metalized Plastic Package
- AC coupled PECL level Inputs
- Low profile fits Mezzanine Card Applications
- Single +3.3V Power Supply
- Wave Solderable / Aqueous Washable
- Class 1 Laser Safety Compliant
- UL 1950 Approved

PRODUCT OVERVIEW

The M2T-25-4-1-L Small Form Factor (SFF) optical dual transmitter modules are high performance integrated duplex data links for uni-directional communication over multimode optical fibre. The M2T-25-4 module is specifically designed to used in Gigabit Etherent/ Fibre

Serializer/De-Serializer

XFT Upgrade

TLK1501
0.6 TO 1.5 GBPS TRANSCEIVER

SLLS428F – JUNE 2000 – REVISED JANUARY 2004

- Hot Plug Protection
- 0.6 to 1.5 Gigabits Per Second (Gbps) Serializer/Deserializer
- High-Performance 64-Pin VQFP Thermally Enhanced Package (PowerPAD™)
- 2.5 V Power Supply for Low Power Operation
- Programmable Voltage Output Swing on Serial Output
- Interfaces to Backplane, Copper Cables, or Optical Converters
- Rated for Industrial Temperature Range
- On-Chip 8-Bit/10-Bit (8B/10B) Encoding/Decoding, Comma Alignment, and Link Synchronization
- On-Chip PLL Provides Clock Synthesis From Low-Speed Reference
- Receiver Differential Input Thresholds 200 mV Minimum
- Typical Power: 250 mW
- Loss of Signal (LOS) Detection
- Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link

Finder Outputs

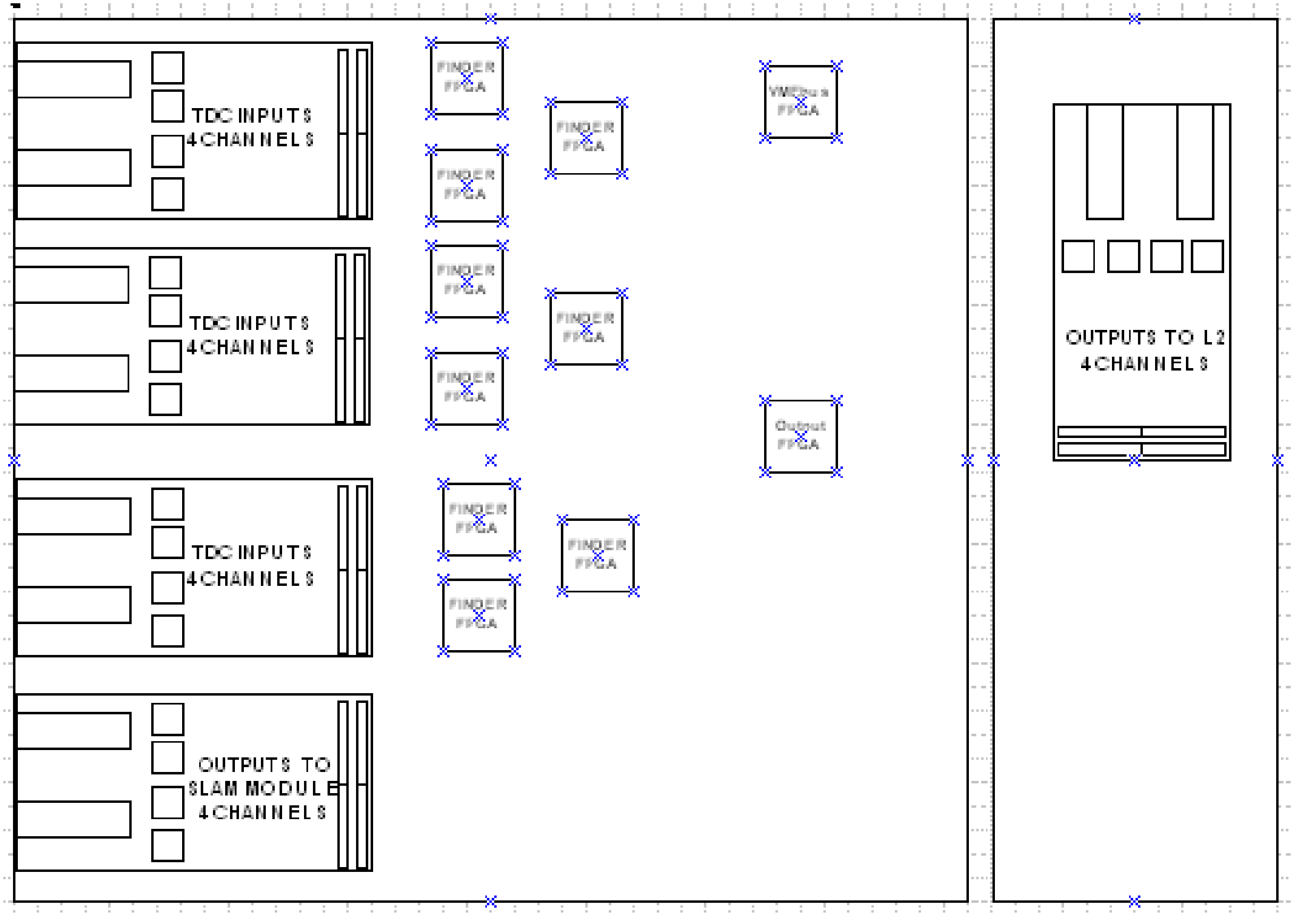
Stereo Finders will output data to L2 and SLAM boards. SLAM boards will have provide inputs to XTRP.

L2 output estimated to be ~120 bytes per board. We will use a link which plugs into the Pulser. Could use Hotlink technology – not determined yet.

SLAM output requires 12bits/cell for each Finder Module. This link will use fiber optic technology similar to TDC->Finder links.

Rough look at layout

XFT Upgrade



Schedule

Stereo Finder Schedule

Finish Schematics	early Sept'04
Finish Layouts	early Oct'04
Preproduction Board under test	early Dec'04
Testing complete	early Mar'05
Production Readiness Review	3/21/05
Production checkout done	late July'05

Estimated Costs

Cost Estimate for Preproduction Stereo Finder

PCB @ $1500

6 dual O/E parts @ $150 = $900

2 dual E/O parts @ $150 = $300

9 Finder FPGAs @ $800 = $7,200 (Altera EP1S25 is ~$865)

1 FPGA general board Control = $250

Misc. logic = $500

5 Mezzanine modules @$300 = $1,500 (possibly put SERDES parts on mezzanine boards)

Board Total = $12,150